FIG. 1A

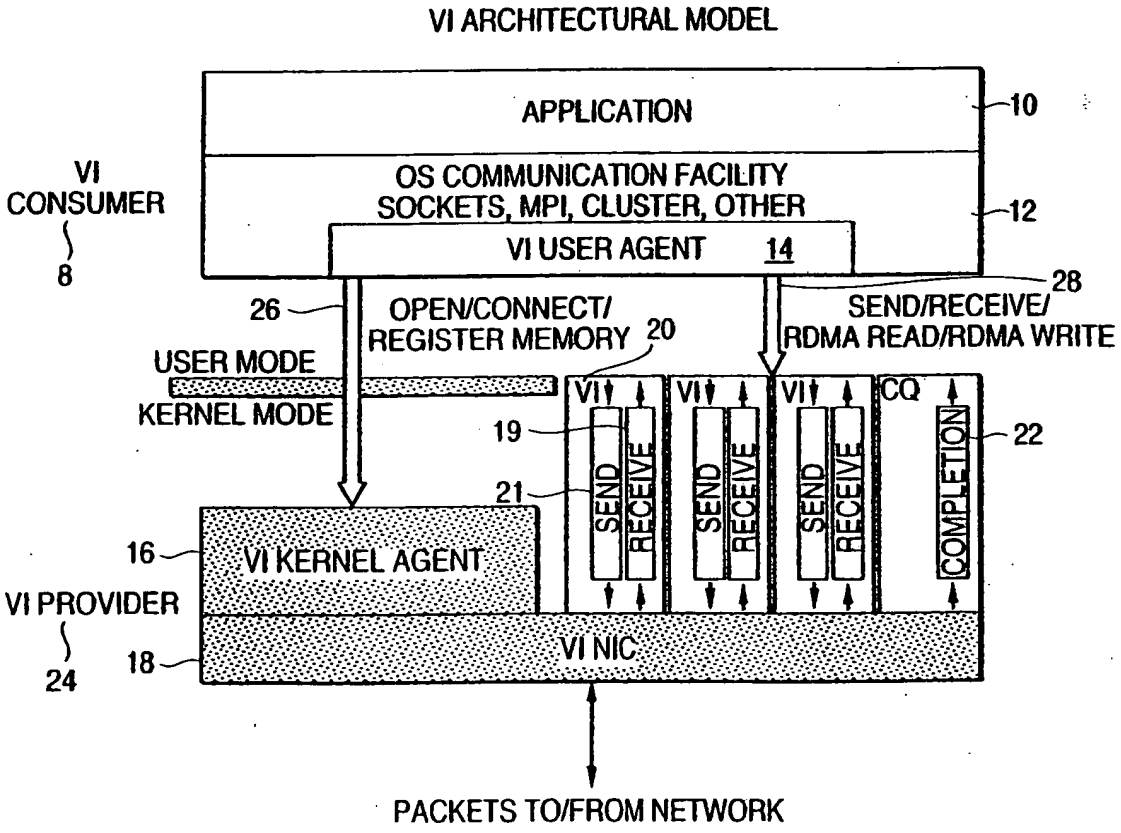
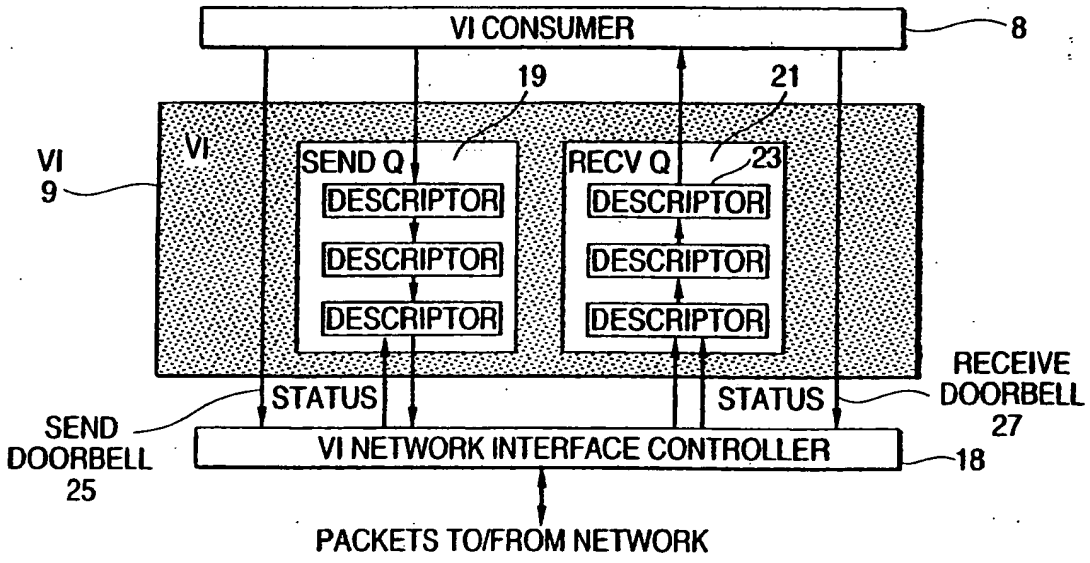

VI ARCHITECTURAL MODEL
APPLICATION
10
VI CONSUMER
8
OS COMMUNICATION FACILITY
SOCKETS, MPI, CLUSTER, OTHER
12
VI USER AGENT 14
26
OPEN/CONNECT/
REGISTER MEMORY
20
28
SEND/RECEIVE/
RDMA READ/RDMA WRITE
USER MODE
KERNEL MODE
VI
VI
VI
CQ
19
22
SEND
RECEIVE
SEND
RECEIVE
SEND
RECEIVE
COMPLETION
21
16
VI KERNEL AGENT
VI PROVIDER
24
18
VI NIC
PACKETS TO/FROM NETWORK

FIG. 1B



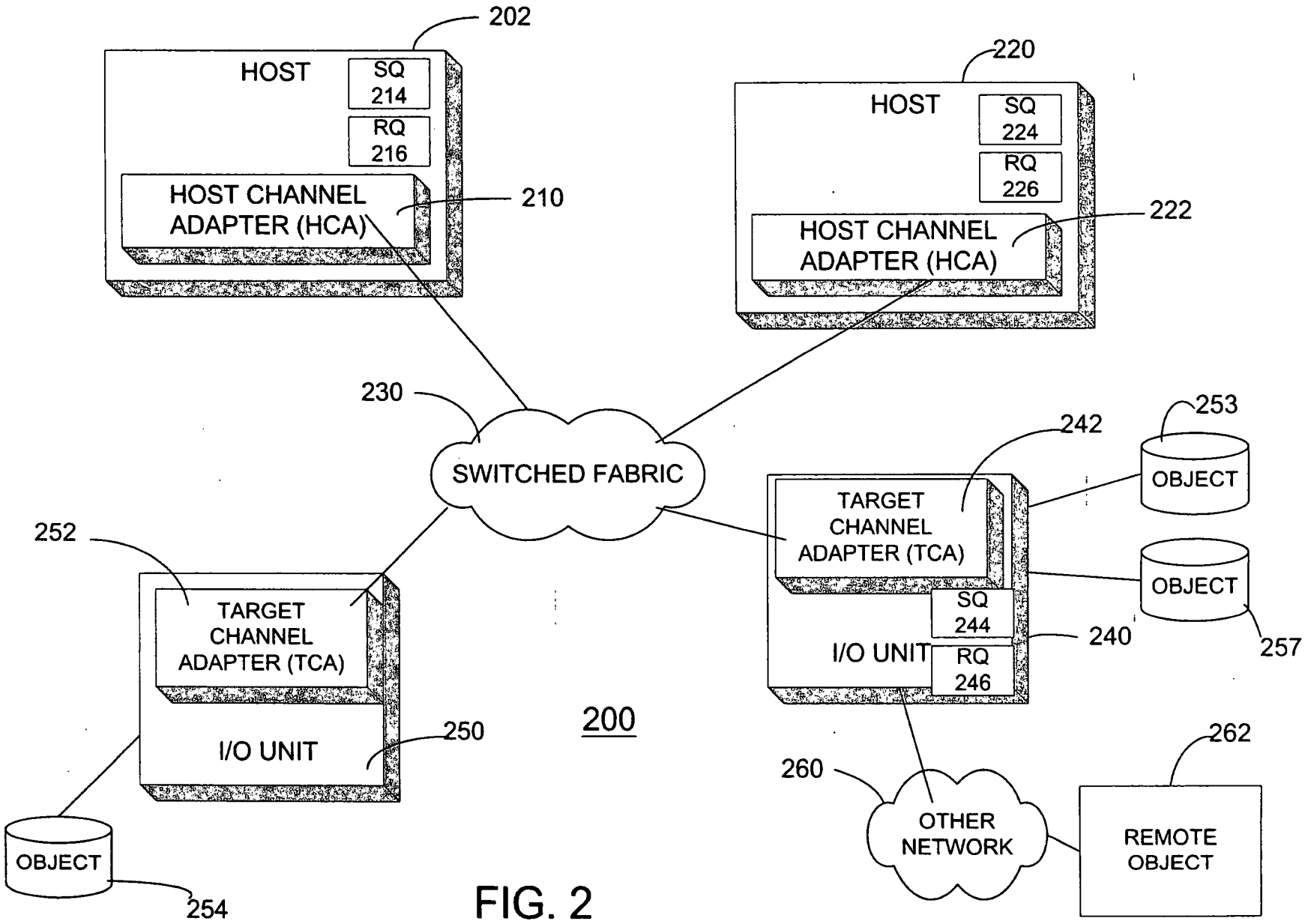
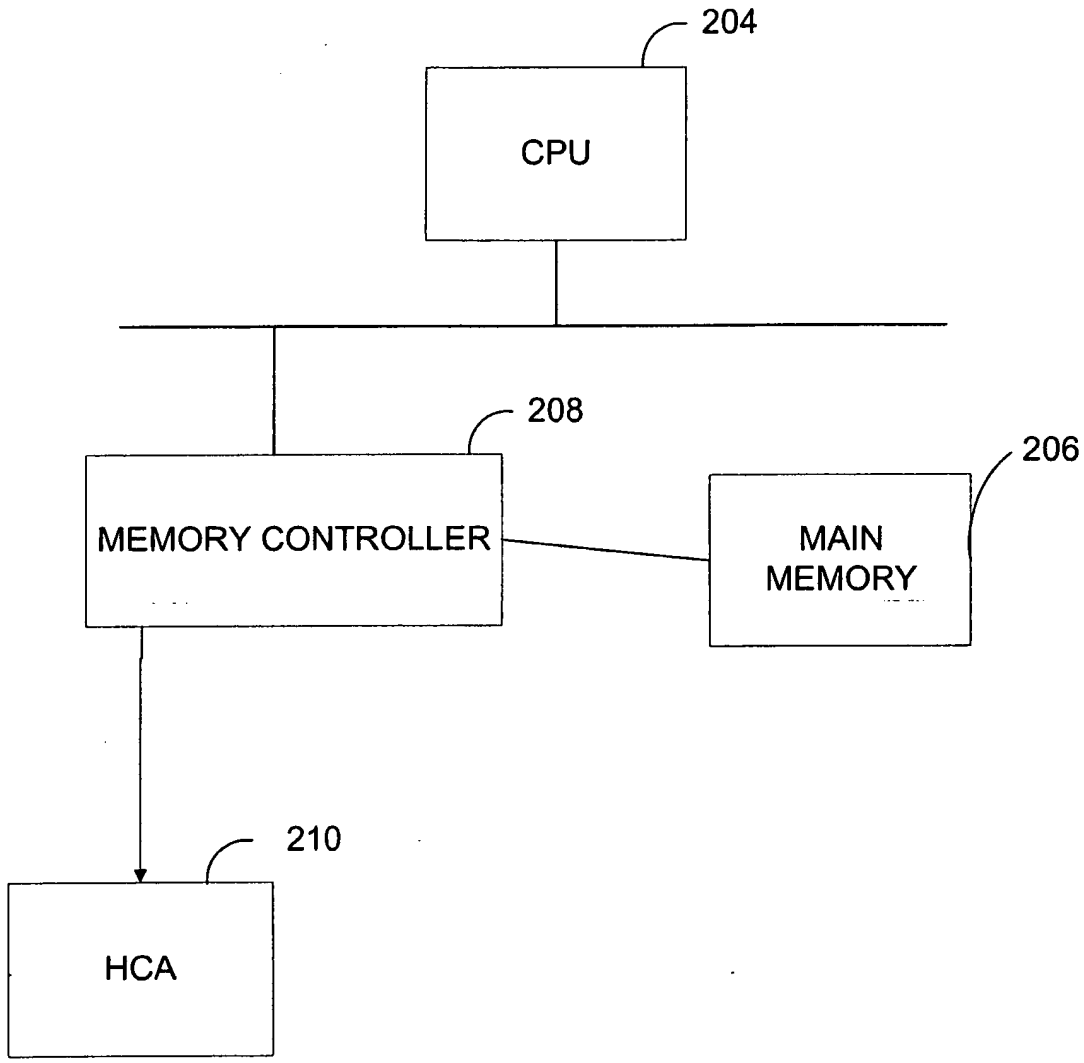


FIG. 2



HOST 202

FIG. 3

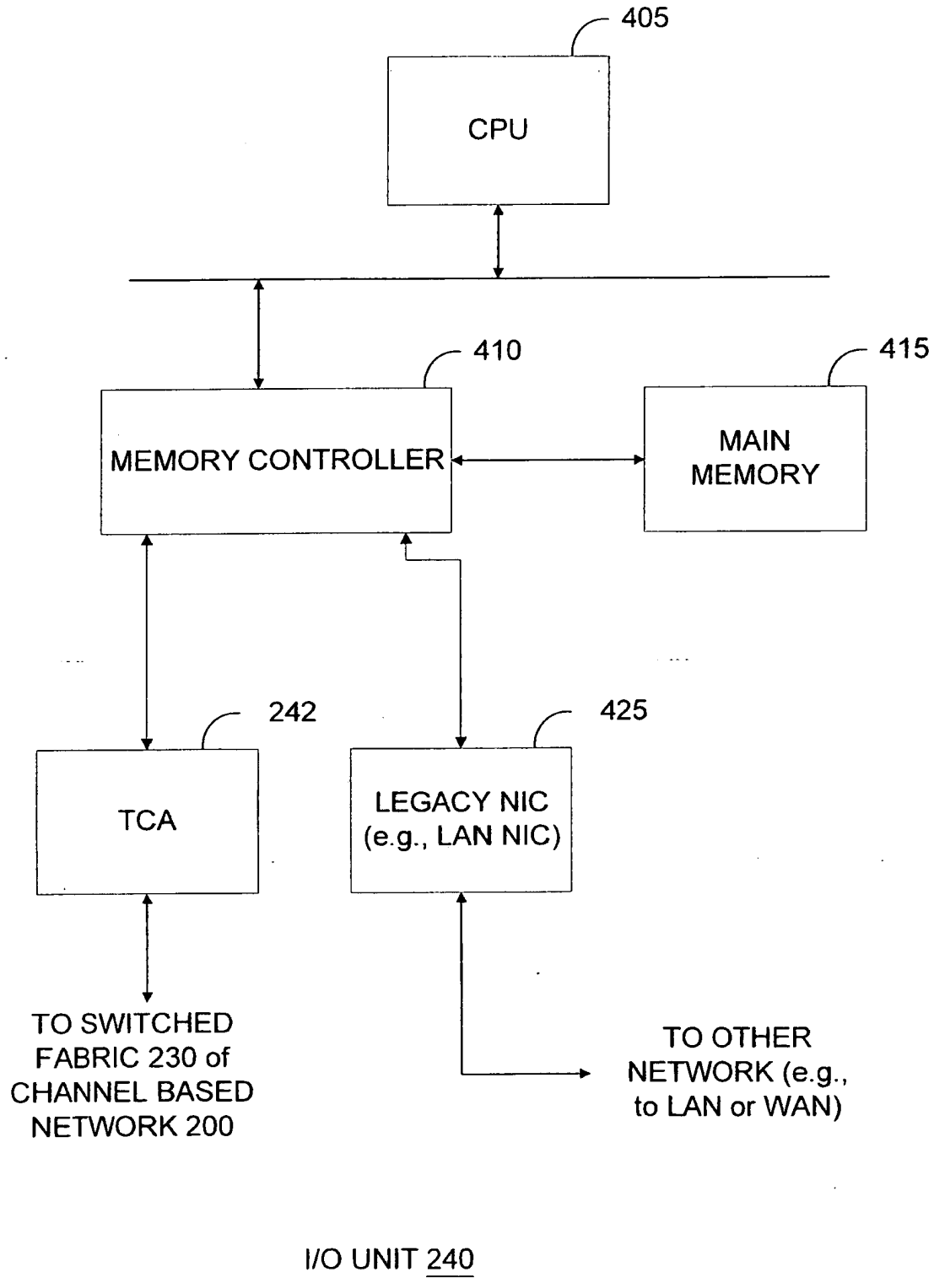
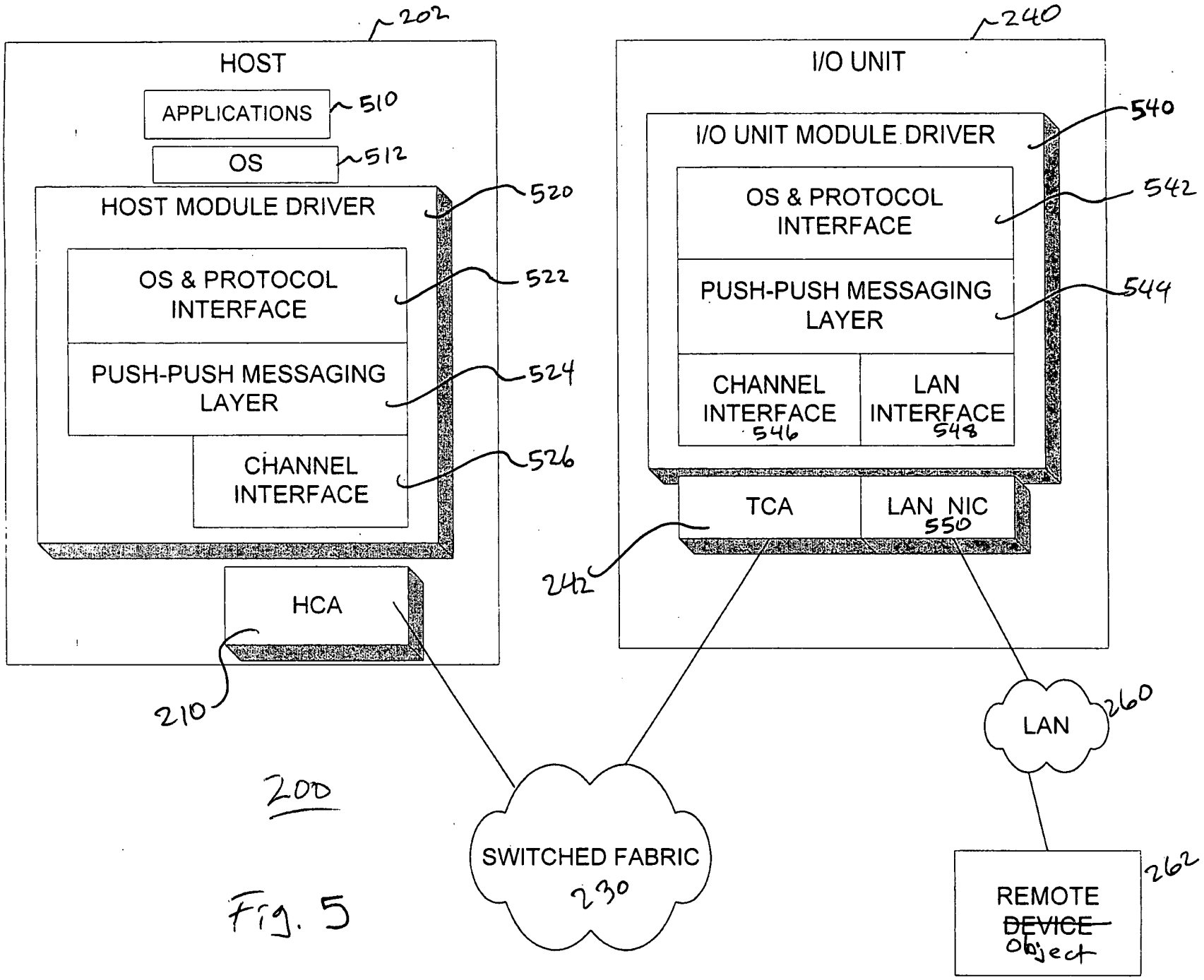
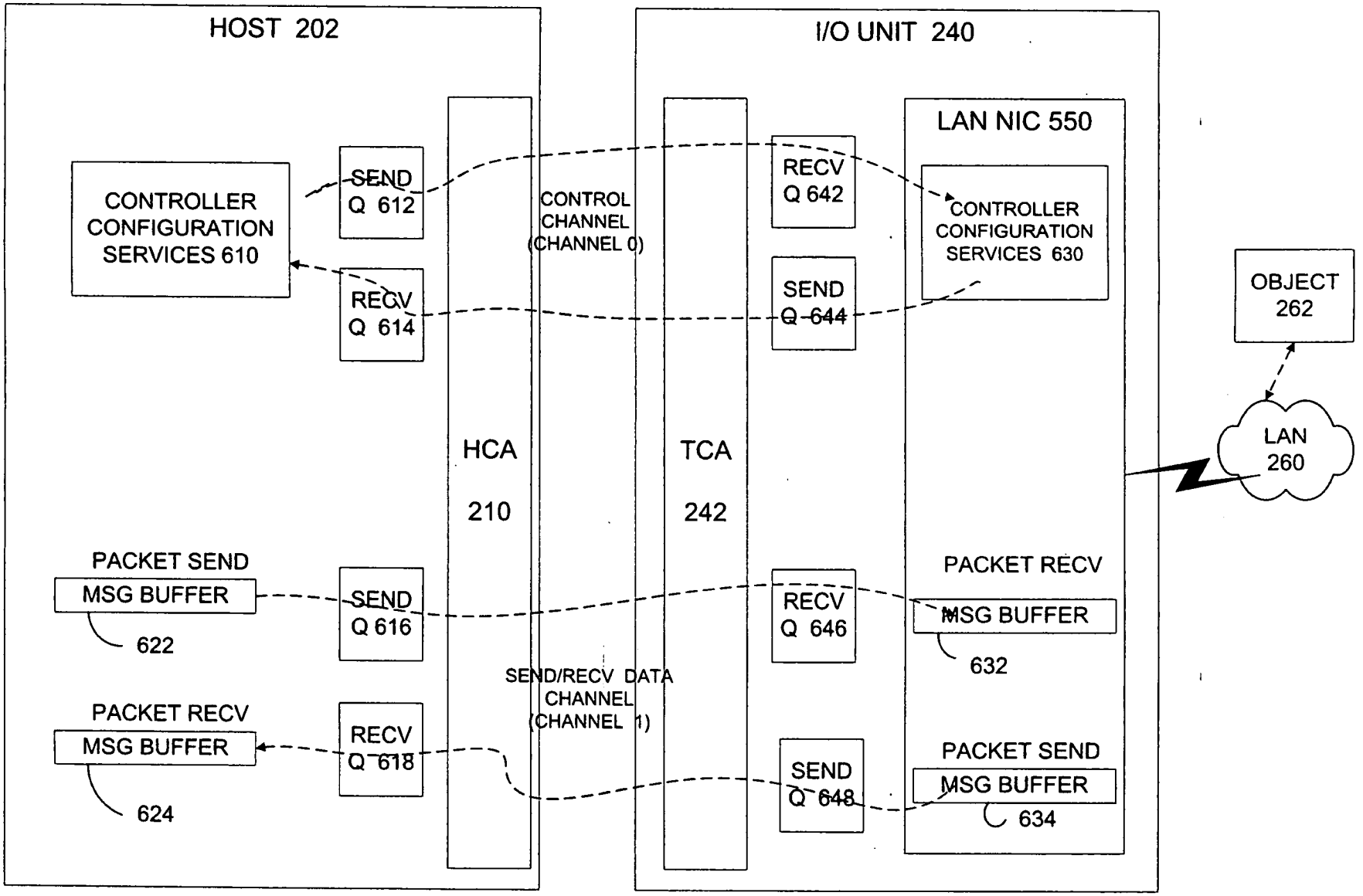

405
CPU
410
415
MEMORY CONTROLLER
MAIN MEMORY
242
425
TCA
LEGACY NIC (e.g., LAN NIC)
TO SWITCHED FABRIC 230 of CHANNEL BASED NETWORK 200
TO OTHER NETWORK (e.g., to LAN or WAN)
I/O UNIT 240

FIG. 4



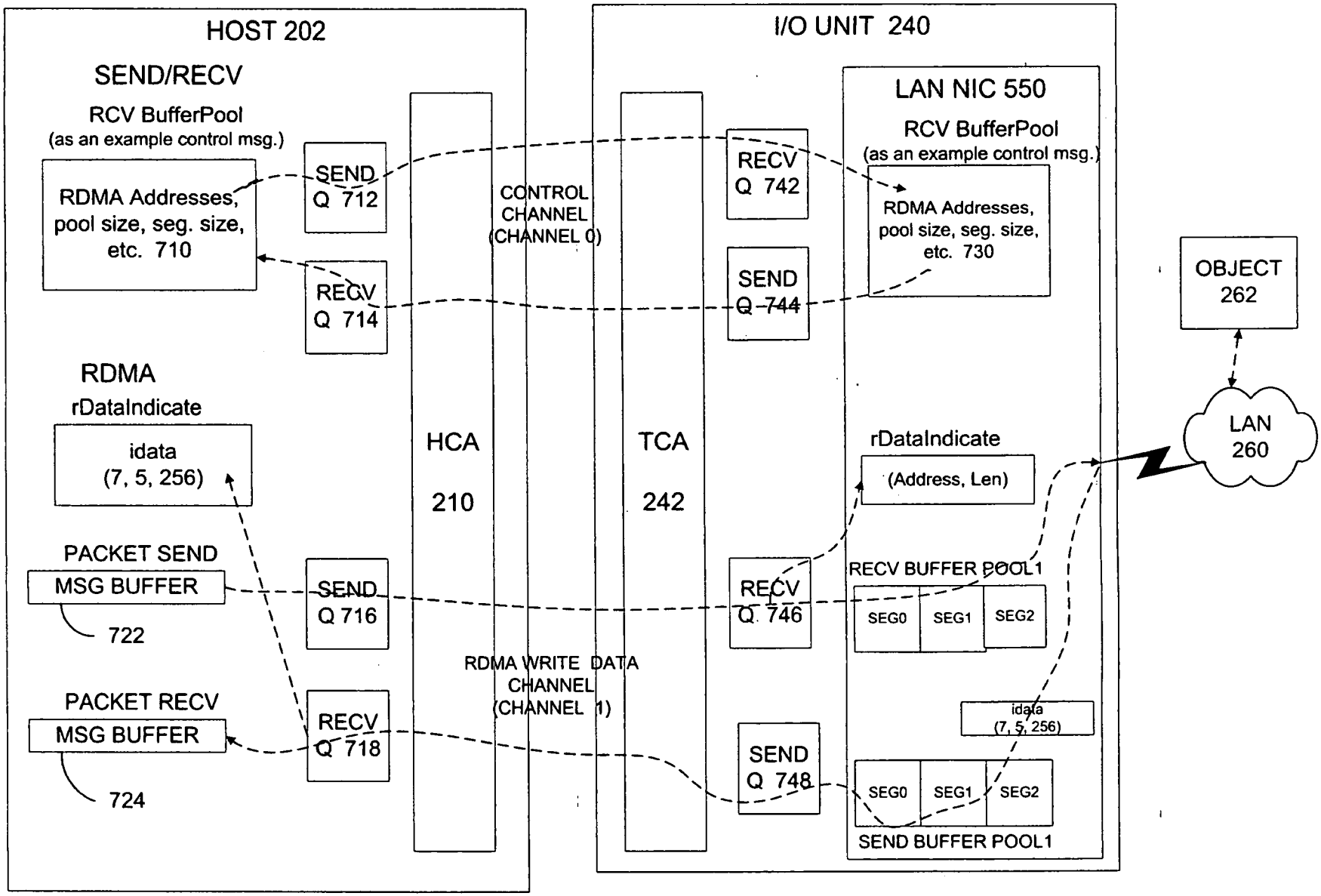
200

Fig. 5



PUSH-PUSH SEND MODEL

FIG. 6



PUSH-PUSH RDMA WRITE MODEL

FIG. 7

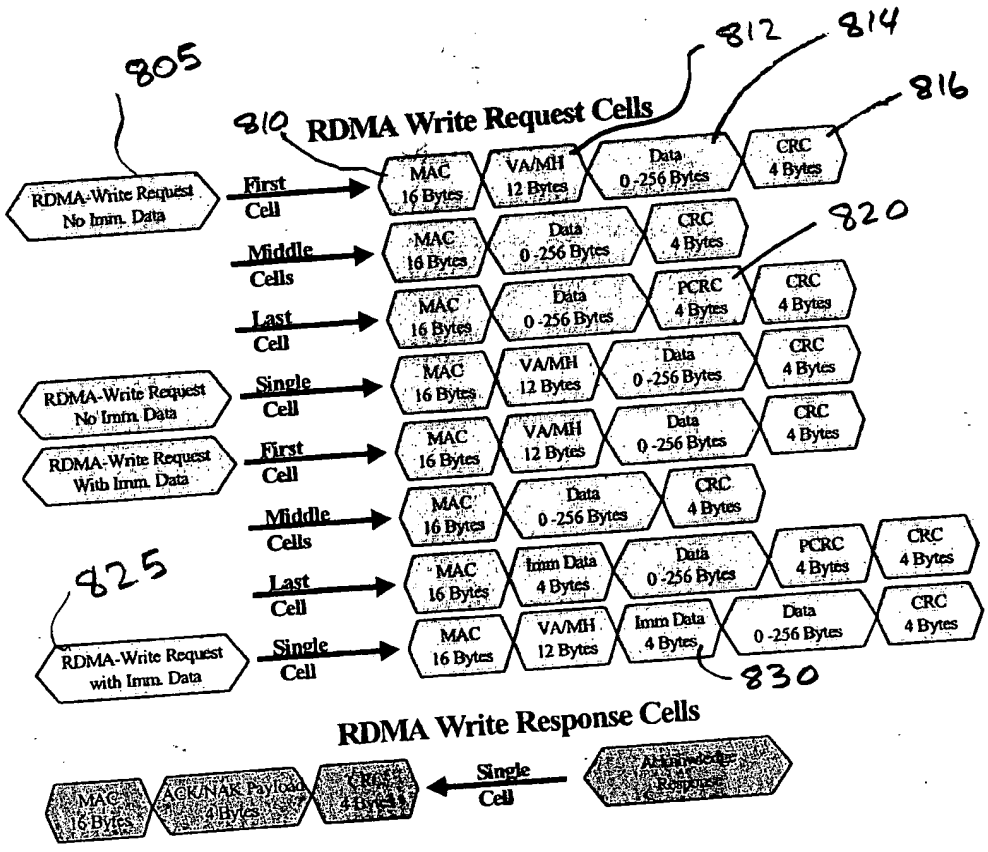

805
810
812
814
816
820
825
830
RDMA Write Request Cells
RDMA-Write Request No Imm. Data
RDMA-Write Request With Imm. Data
RDMA-Write Request with Imm. Data
First Cell
Middle Cells
Last Cell
Single Cell
MAC 16 Bytes
VA/MH 12 Bytes
Data 0 -256 Bytes
CRC 4 Bytes
PCRC 4 Bytes
Imm Data 4 Bytes
RDMA Write Response Cells
Single Cell
MAC 16 Bytes
ACK/NAK Payload 4 Bytes
CRC 4 Bytes

Fig. 8